

ETCH BACK OF INTERCONNECT DIELECTRICS

BACKGROUND OF THE INVENTION

5 This invention relates to an etch back of the interconnect dielectric to improve electrical and mechanical reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-section view of a semiconductor wafer in accordance with the present
10 invention.

FIG. 2 is a cross-section view of a semiconductor wafer in accordance with another embodiment of the present invention.

FIG. 3 is a flow diagram illustrating the process flow of the present invention.

FIGS. 4A-4F are cross-sectional views of a partially fabricated semiconductor wafer
15 in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will now be described with reference to the attached drawings, wherein like reference numerals are used to refer to like elements throughout. Several
20 aspects of the invention are described below with reference to example applications for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide a full understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details or with other methods. In other instances, well-known

structures or operations are not shown in detail to avoid obscuring the invention. The figures are not drawn to scale; they are provided merely to illustrate the present invention.

Referring to the drawings, FIG. 1 depicts a best mode application of the present
5 invention. FIG. 1 shows a cross section of a portion of a semiconductor wafer 4. The example semiconductor wafer 4 is divided into two sections: a front-end module 5, and a back-end module 6. It is within the scope of the invention to have any form of logic within the front-end module. The example logic contained in the partial semiconductor wafer 4 is a transistor formed in the substrate 7 that has source/drain 8, 9 and gate 10. Any one of a
10 number of isolation structures 11 is used adjacent to the transistor to electrically separate the transistors from each other. Immediately above the transistor is a layer of insulation 12 containing metal contacts 13 which electrically tie the transistor to the other logic elements (not shown) of the front-end structure 5. As an example, insulation 12 may be SiO₂ and metal contacts 13 may comprise W.

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The back-end module 6 contains one or more metal or via layers 14, 15, 16. Each metal or via layer contains interconnects. The interconnects may be metal lines 17, 19 that route electrical signals and power properly through the electronic device. In addition, the interconnects may be vias 18 that properly connect the metal lines 17 of a first metal layer 14
20 to the metal lines 19 of a second metal layer 16. As an example, the interconnects 17, 18, 19 may be comprised of a metal such as copper.

The interconnects are electrically insulated by any one of a number of dielectric materials 20. In the example application, the dielectric insulation 20 is a low-k material such as Organo-Silicate Glass (“OSG”).

5 In addition, there is a thin dielectric layer 21 formed between the dielectric regions
20. It is within the scope of this invention to use any suitable material for the dielectric layer
21. For example, the dielectric layer 21 may comprise SiC. The use of a dielectric layer 21 is
optional; however, the dielectric layer 21 may perform many functions. For example,
dielectric layer 21 may function as a barrier layer; preventing the diffusion of copper from
10 interconnects 17 to either the silicon channel of the transistor or another isolated metal line
(thereby creating an electrical short). Second, dielectric layer 21 may function as an etch stop
when forming the features within the dielectric insulation 20 during manufacturing to
eventually create the interconnects 17, 18, 19. Lastly, the dielectric layer 21 may function as
an adhesion layer to help hold a layer of OSG 20 to a metal interconnect 17, 18, 19. For
15 purposes of readability, the dielectric layer 21 will be called the barrier layer 21 during the
rest of the description of this invention.

As shown in FIG. 1, the edges of the metal lines 17, 19 and vias 18 are often not fully landed or aligned correctly. Therefore, there are numerous sharp corners 22 at the top or
20 bottom surfaces of the interconnects 17, 18, 19. These corners 22 are high electrical field stress points. When corners 22 are adjacent to the interface between the dielectric 20 and the barrier 21, the electrical breakdown strength of the interconnects 17, 18, 19 is reduced. Therefore, in the best mode application, the corners 22 are offset from any dielectric-barrier interface 20, 21. Thus the reliability of the electrical circuit is improved because the

proximity of the dielectric-barrier interface 20, 21 is offset from the high field stress region of the interconnects 17, 18, 19.

Referring again to the drawings, FIG. 2 shows another implementation of the present invention. FIG. 2 shows a cross section of a portion of a semiconductor wafer 4 that is similar to the semiconductor wafer 4 of FIG. 1. (Similar reference numerals are used throughout the figures to designate like or equivalent features.) However, the semiconductor wafer 4 in FIG. 2 does not contain the barrier layer 21. Therefore, in accordance with the invention, the corners 22 of interconnects 17, 18, 19 are located within the bulk of the dielectric portion 20 of the adjacent metal or via layer (i.e. via layer 15 and metal layer 16).

Referring again to the drawings, FIG. 3 is a flow diagram illustrating the process flow of the best mode embodiment of the present invention. Other than process step 312 and possibly process step 310, the front-end and back-end process steps should be those standard in the industry. The present invention may be used in any integrated circuit configuration; therefore (step 200) the front-end module 5 may be fabricated to perform any device function.

Next the first metal layer 14 is fabricated over the front-end module 5. Referring now to FIGS. 3 and 4A-D, a barrier layer 21 may be formed (step 300) over the entire substrate. (It is within the scope of this invention to omit the barrier layer 21 from the back end module.) Next a dielectric layer 20 is formed (step 302, FIG. 4A) over the entire substrate (i.e. over the barrier layer 21, if present). The barrier layer 21 and the dielectric layer 20 may be formed using any manufacturing process such as Chemical Vapor Deposition (“CVD”). In this example application, the barrier layer 21 is comprised of SiC and the dielectric layer 20 is

comprised of OSG; however, any dielectric material may be used. The barrier layer 21 (if present) and the dielectric layer 20 are then patterned and etched (step 304, FIG. 4B) to form holes for the metal interconnects.

5 A metal layer 17 is now formed (step 306, FIG. 4C) over the substrate. In the best mode application, the metal layer is copper; however, the use of other metals such as aluminum or titanium are within the scope of this invention. The metal layer 17 is now polished (step 308, FIG. 4D) until the top surface of the dielectric 20 is exposed and the metal interconnects 17 are formed. In the best mode application, step 308 is performed using a
10 10 Chemical Mechanical Polish (“CMP”); however, other manufacturing techniques may be used.

A wet clean (step 310) may now be performed and may use deionized water or acid. However, it's likely that harmful post-CMP residue will remain on the surface of the
15 15 semiconductor wafer even after the wet clean process. This residue may consist of leftover slurry (i.e. tungsten or silicon oxide balls), carbon particles (which are attracted to the porous low-k dielectric material 20), or slurry packed into surface recesses created by the CMP process. This harmful post-CMP residue weakens the adhesion of subsequent material layers and also reduces the electrical breakdown strength of the back-end module.

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In accordance with the best mode application, the dielectric 20 between the copper interconnects 17 is etched (step 312, FIG. 4E) so that the top surface of the dielectric 20 is lower than the top surface of the copper interconnects 17. As an example, the top surface of the dielectric 20 may be 10-30% below the top surface of the interconnects 17. This etch step

removes the harmful post-CMP residue and also lowers the interface of dielectric 20 from the high electric field corners 22 of the interconnects 17.

The etch step 312 may be a plasma etch that is similar to the standard plasma etch
5 used to etch barrier dielectric material. However, the use of any dielectric etch is within the scope of this invention. The etch is selective to the film the etch lands on. For example, the etch of step 312 may be a silicon carbide etch or a silicon nitride etch. Moreover, step 312 may be performed using the wet clean process of step 310 to recess the dielectric regions 20 plus a solvent that removes the remaining post-CMP residue. The first metal layer 14 is now
10 complete.

An optional barrier layer 21 may now be formed (step 314, FIG. 4F) over the semiconductor substrate. The barrier layer 21 may comprise any dielectric material, such as SiC. Now the fabrication any remaining metal layers 15, 16 of the back-end module
15 continues (step 316) until the back-end module is complete. Referring back to FIG. 1, the completed back-end module may contain one or more metal layers 14, 15, 16 to be used as vias or signal and power lines. Moreover, the present invention may be used in any location throughout the back-end module.

If a barrier layer 21 is used, then the interface between the dielectric 20 and the barrier 21 will be below the highest electric field stress point corner 22 (as shown in FIG. 1). If a barrier layer 21 is not used, then the interface between the dielectric material 20 of adjoining metal layers 14, 15, 16 is also recessed from the corners 22 of the interconnects 17, 18, 19 (as shown in FIG. 2).

Various modifications to the invention as described above are within the scope of the claimed invention. As an example, instead of OSG, the dielectric material 20 may be aerogel, BLACK DIAMOND, xerogel, SiLK, or HSQ. Similarly, instead of SiC, the barrier material 5 21 may be silicon nitride, silicon oxide, nitrogen-doped silicon carbide, or oxygen doped silicon carbide. The metal interconnects 17, 18, 19 may be comprised of any suitable metal, such as Cu, W, or Al. In addition, it is within the scope of the invention to have a back-end module structure 6 with a different amount or configuration of metal layers 14, 15, 16 than is shown in FIGS. 1 and 2. Furthermore, the invention is applicable to semiconductor wafers 10 having different front-end well and substrate technologies, transistor configurations, and metal connector materials or configurations. Moreover, the invention is applicable to other semiconductor technologies such as BiCMOS, bipolar, SOI, strained silicon, pyroelectric sensors, opto-electronic devices, microelectrical mechanical system (“MEMS”), or SiGe.

15 While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Numerous changes to the disclosed embodiments can be made in accordance with the disclosure herein without departing from the spirit or scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above described 20 embodiments. Rather, the scope of the invention should be defined in accordance with the following claims and their equivalents.